Introduction to Digital Logic

EECS/CSE 31L

**Assignment 4: Register**

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**1 Block Description**

* Construct a register that can be parameterized
* Can load a given input value
* Increment the value stored in the register
* Has an asynchronous reset and synchronous reset

**2 Input/Output Port Description**

|  |  |  |  |
| --- | --- | --- | --- |
| Generic Name | Data Type | Default Value | Description |
| NBIT | INTEGER | 32 | Size of register |

|  |  |  |  |
| --- | --- | --- | --- |
| Port name | Port size | Port Type | Description |
| Clk | 1 | IN | Triggers the register process |
| Rst\_a | 1 | IN | Will reset the register when active |
| Rst\_s | 1 | IN | Will reset the register when active and clock rises |
| We | 1 | IN | Enables writing to the register |
| din | NBIT-1 downto 0 | IN | The input value |
| dout | NBIT-1 downto 0 | OUT | The register’s stored value |

|  |  |  |  |
| --- | --- | --- | --- |
| Variable Name | Data Type | Port size | Description |
| temp | INTEGER | NBIT-1 downto 0 | Aids in register process |

**3 Design Schematics**

**Truth Table:**

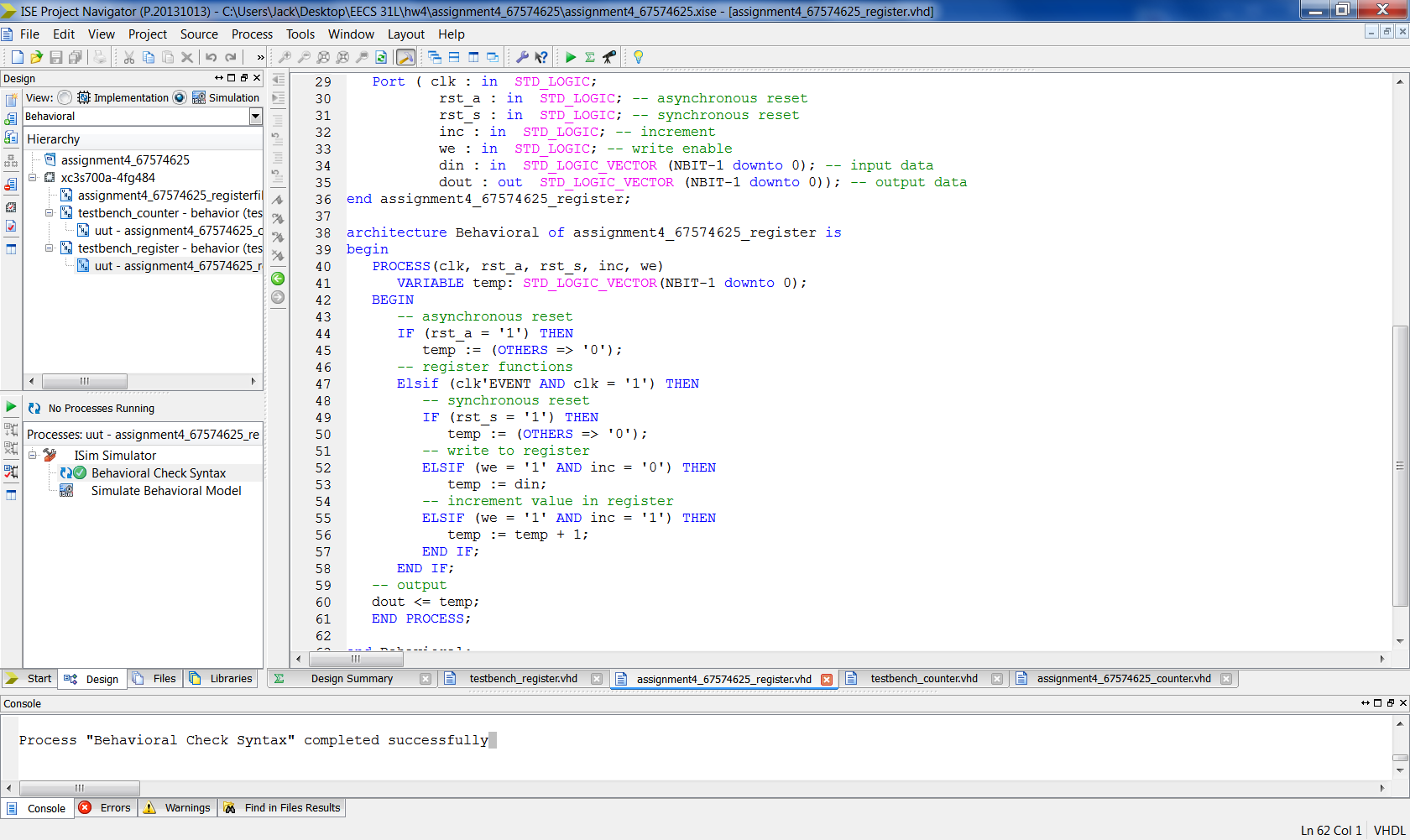
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Clk (Rising edge) | Rst\_a | Rst\_s | inc | we | Function |
| X | 1 | X | X | X | Asynchronous Reset |
| 1 | 0 | 1 | X | X | Synchronous Reset |
| 1 | 0 | 0 | 0 | 1 | Load Input |
| 1 | 0 | 0 | 1 | 1 | Increment Value Stored in Register |

**Design:**

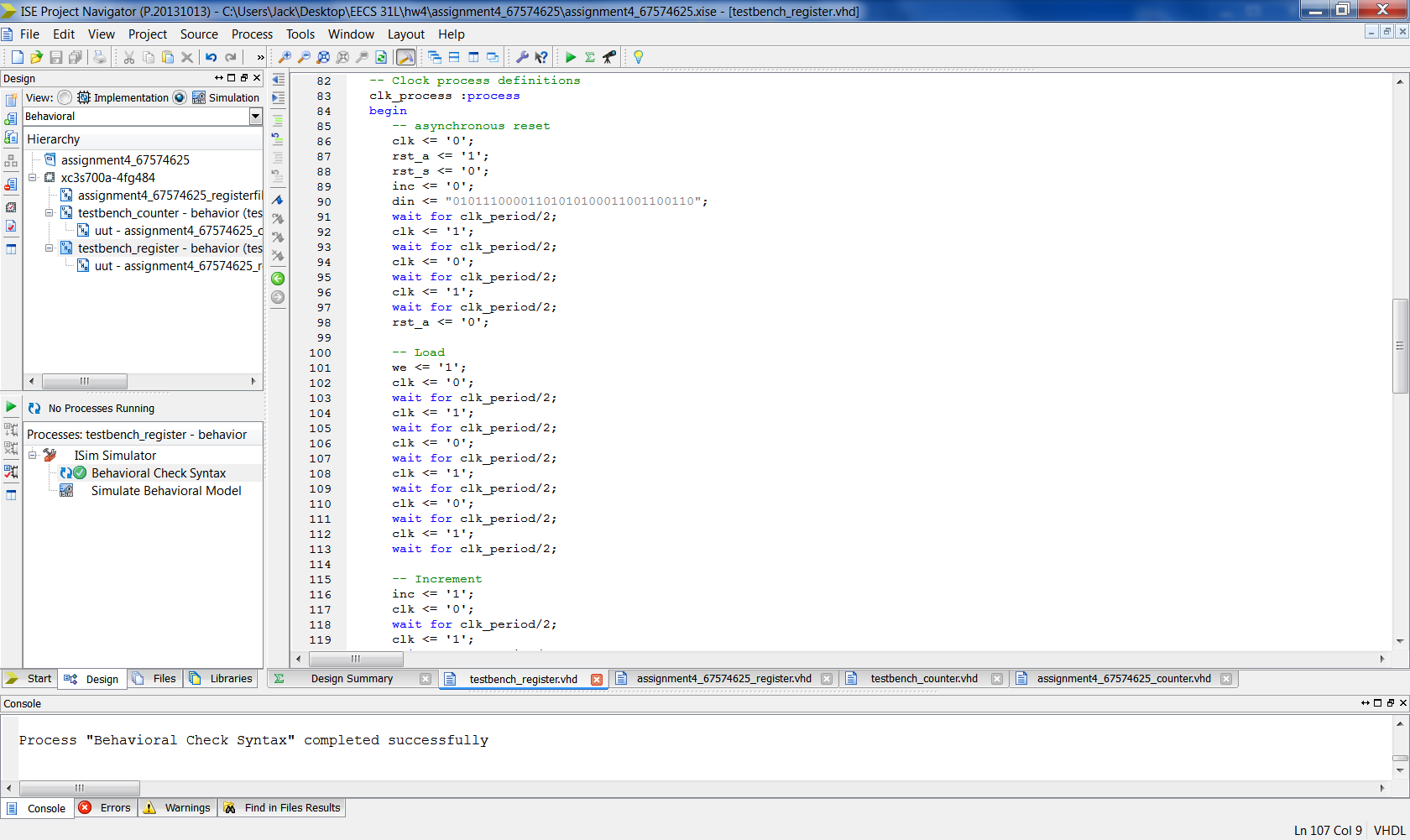


**4 Compilation**

Register



Testbench



**5 Elaboration**

**Assumptions:**

* Register can store any NBIT value

Regarding how I wrote my vhdl code

* I used a process with a variable called temp
* Used sequential if and elsif statements

**Errors and Challenges:**

* I was having issues early on with the process statement. I didn’t realize “else if” id “elsif” in VHDL
* Misusing assignment operators; tried using signal assignment operator on a variable

**Simulation Log:**

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register\_beh.prj} work.testbench\_register {}

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register\_isim\_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register\_beh.prj work.testbench\_register

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/assignment4\_67574625\_register.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling package std\_logic\_arith

Compiling package std\_logic\_unsigned

Compiling package numeric\_std

Compiling architecture behavioral of entity assignment4\_67574625\_register [\assignment4\_67574625\_register(3...]

Compiling architecture behavior of entity testbench\_register

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 8 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register\_isim\_beh.exe

Fuse Memory Usage: 37152 KB

Fuse CPU Usage: 529 ms

Launching ISim simulation engine GUI...

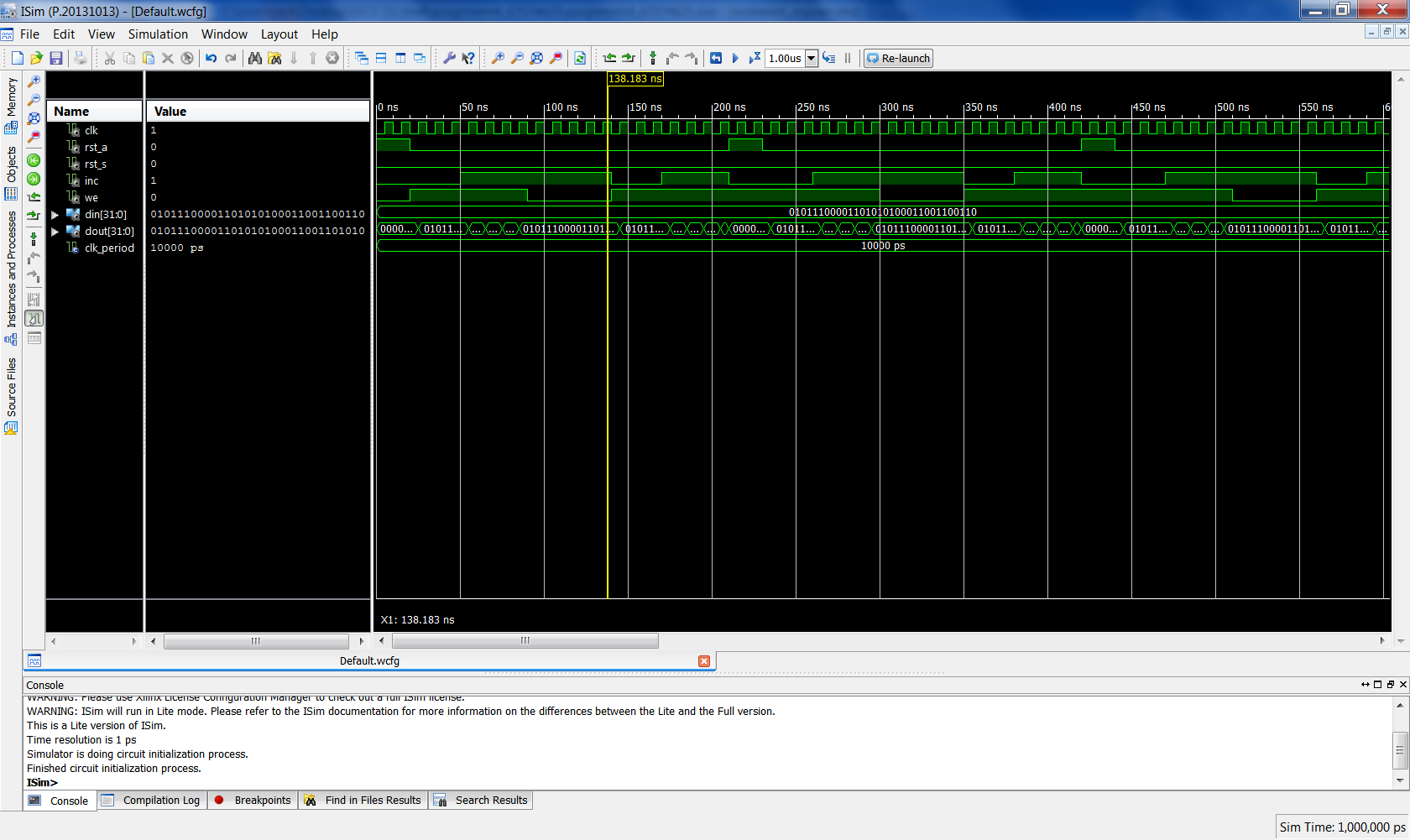
"C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4\_67574625/testbench\_register\_isim\_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

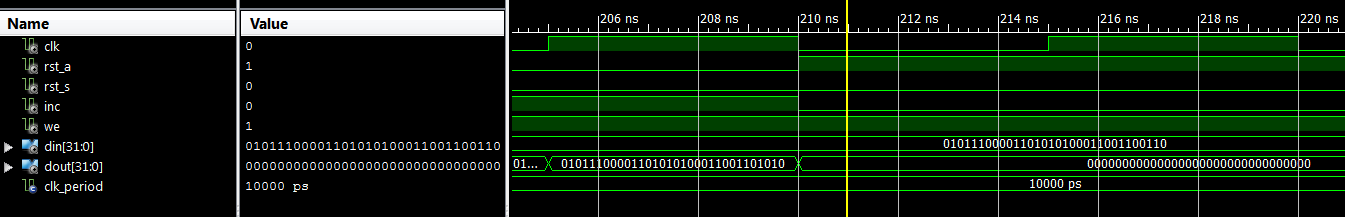
**6 Waveforms**

*Full Waveform Snapshot*

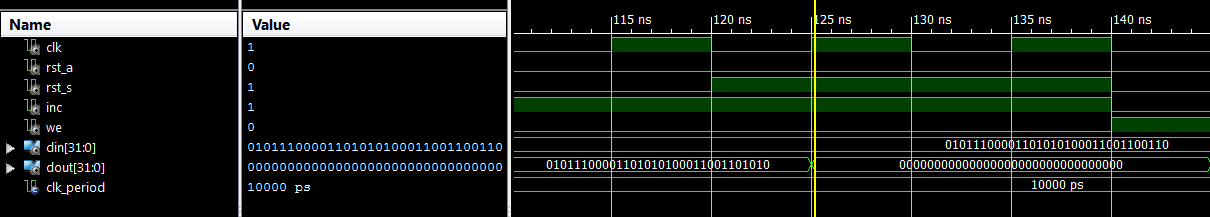


*Snapshots of Waveform*

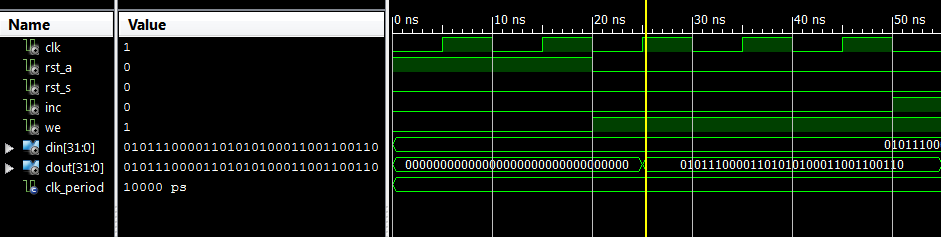
Reset (asynchronous)



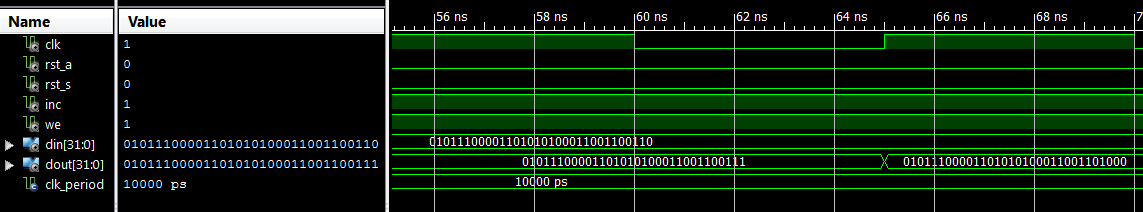
Reset (synchronous)



Load input



Increment



Hold (write enable off)

